WE CLAIM:

1. A semiconductor integrated circuit capacitor, comprising:

an insulating substrate;

a lower electrode disposed on a predetermined part of the insulating substrate;

an interlevel insulating layer disposed on the insulating substrate and on the lower electrode;

a via hole having sidewalls, whereby the via hole passes through the interlevel insulating layer and exposes a predetermined surface of the lower electrode;

a spacer diposed on the sidewalls of the via hole;

a dielectric layer disposed on: (i) a bottom surface of the via hole adjacent to the predetermined surface of the lower electrode; (ii) a predetermined part of the insulating layer; and (iii) the spacer; and

an upper electrode disposed on a predetermined part of the interlevel insulating layer and disposed on the dielectric layer.

2. The capacitor as claimed in claim 1, wherein the spacer is made from a conductive layer comprising a tungsten containing material.

3. The capacitor as claimed in claim 1, wherein the dielectric layer has a structure selected from: (i) a single-level structure containing an oxide layer or nitride layer; or (ii) a multi-level structure containing layers selected from the group consisting of oxide layers, nitride layers, and mixtures thereof.

4. The capacitor as claimed in claim 3, wherein the oxide layer is made using a deposition technique employing Plasma Enhanced Oxide (PEOX), P-SiH_4, or High Density Plasma (HDP).

5. The capacitor as claimed in claim 3, wherein the nitride layer is made using a deposition technique employing Plasma Enhanced Nitride (PESiN).

6. The capacitor as claimed in claim 3, wherein the multi-level structure is selected from the group consisting of an oxide/nitride layer, a nitride/oxide layer, an oxide/nitride/oxide layer and a nitride/oxide/nitride layer.

7. The capacitor as claimed in claim 1, wherein the lower and upper electrodes are made of a material selected from an aluminum alloy, a copper alloy, and mixtures thereof.

8. The capacitor as claimed in claim 7, further comprising an anti-reflection layer disposed on the lower and/or upper electrodes' surface.

9. The capacitor as claimed in claim 8, wherein the anti-reflection layer has a structure selected from the group consisting of: (i) a single-level structure comprised of one or more materials selected from the group consisting of Ti, Ta, W, Mo, TiN, TiW, TaN, and MoN; (ii) a multi-level structure comprised of one or more materials selected from the group consisting of W-Si-N, Ta-Si-N, W-B-N, and Ti-Si-N; and (iii) mixtures thereof.

10. The capacitor as claimed in claim 7, further comprising a metal barrier layer disposed on the lower and/or upper electrodes's surface.

11. The capacitor as claimed in claim 10, wherein the metal barrier layer has a structure selected from the group consisting of: (i) a single-level structure comprised of one or more materials selected from the group consisting of Ti, Ta, W, Mo, TiN, TiW, TaN, and MoN; (ii) a multi-level structure comprised of one or more materials selected from the group consisting of W-Si-N, Ta-Si-N, W-B-N, and Ti-Si-N; and (iii) mixtures thereof.

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12. A method of making a semiconductor integrated circuit capacitor, comprising:

providing an insulating substrate;

simultaneously forming a first wire line and a lower electrode on predetermined surfaces of the insulating substrate;

forming an interlevel insulating layer on the substrate, on the first wire line, and on the lower electrode;

selectively etching the interlevel insulating layer to expose a predetermined surface of the lower electrode and a predetermined surface of the first wire line thereby simultaneously forming in the interlevel insulating layer: (i) a first via hole having sidewalls and disposed above the lower electrode; and (ii) a second via hole disposed above the first wire line;

forming a conductive layer on the interlevel insulating layer and in the first and second via holes;

etching back the conductive layer to form: (i) a spacer on the sidewalls of the first via hole; (ii) a conductive plug in the second via hole; and (iii) an exposed surface containing the spacer, conductive plug, the predetermined surface of the lower electrode, and predetermined surfaces of the interlevel insulating layer;

forming a dielectric layer on the exposed surface;

removing the dielectric layer on the exposed surface except for a predetermined portion of the dielectric layer disposed on the spacer and predetermined surface of the lower electrode; and

simultaneously forming: (i) a second wire line connected to the conductive plug; and (ii) an upper electrode connected to the dielectric layer.

13. The method as claimed in claim 12, wherein the spacer is made from a conductive layer comprising a tungsten containing material.

14. The method as claimed in claim 12, wherein the dielectric layer has a structure selected from: (i) a single-level structure containing an oxide layer or nitride layer; or (ii) a multi-level structure containing layers selected from the group consisting of oxide layers, nitride layers, and mixtures thereof.

15. The method as claimed in claim 14, wherein the oxide layer is made using a deposition technique employing Plasma Enhanced Oxide (PEOX), P-SiH$_4$, or High Density Plasma (HDP).

16. The method as claimed in claim 14, wherein the nitride layer is made using a deposition technique employing Plasma Enhanced Nitride (PESiN).

17. The method as claimed in claim 14, wherein the multi-level structure is selected from the group consisting of an oxide/nitride layer, a nitride/oxide layer, an oxide/nitride/oxide layer and a nitride/oxide/nitride layer.

18. The method as claimed in claim 12, wherein the lower and upper electrodes are made of a material selected from an aluminum alloy, a copper alloy, and mixtures thereof.

19. The method as claimed in claim 18, further comprising an anti-reflection layer disposed on the lower and/or upper electrodes' surface.

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~~20. The method as claimed in claim 19, wherein the anti-reflection layer has a structure selected from the group consisting of: (i) a single-level structure comprised of one or more materials selected from the group consisting of Ti, Ta, W, Mo, TiN, TiW, TaN, and MoN; (ii) a multi-level structure comprised of one or more materials selected from the group consisting of W-Si-N, Ta-Si-N, W-B-N, and Ti-Si-N; and (iii) mixtures thereof.~~

21. The method as claimed in claim 18, further comprising a metal barrier layer disposed on the lower and/or upper electrodes's surface.

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~~22. The method as claimed in claim 21, wherein the metal barrier layer has a structure selected from the group consisting of: (i) a single-level structure comprised of one or more materials selected from the group consisting of Ti, Ta, W, Mo, TiN, TiW, TaN, and MoN; (ii) a multi-level structure comprised of one or more materials selected from the group consisting of W-Si-N, Ta-Si-N, W-B-N, and Ti-Si-N; and (iii) mixtures thereof.~~

23. The method as claimed in claim 12, further comprising, after forming the first and second via holes, RF sputter etching the interlevel insulating layer and the first and second via holes.

24. The method as claimed in claim 12, wherein the interlevel insulating layer is selectively etched by a process selected from the group consisting of dry-etching, wet-etching and dry/wet-combined etching.

~~25. The capacitor as claimed in claim 1, wherein the spacer disposed on the sidewalls of the via hole has a sloping surface.~~

26. The method as claimed in claim 12, wherein the spacer formed on the sidewalls of the via hole has a sloping surface.